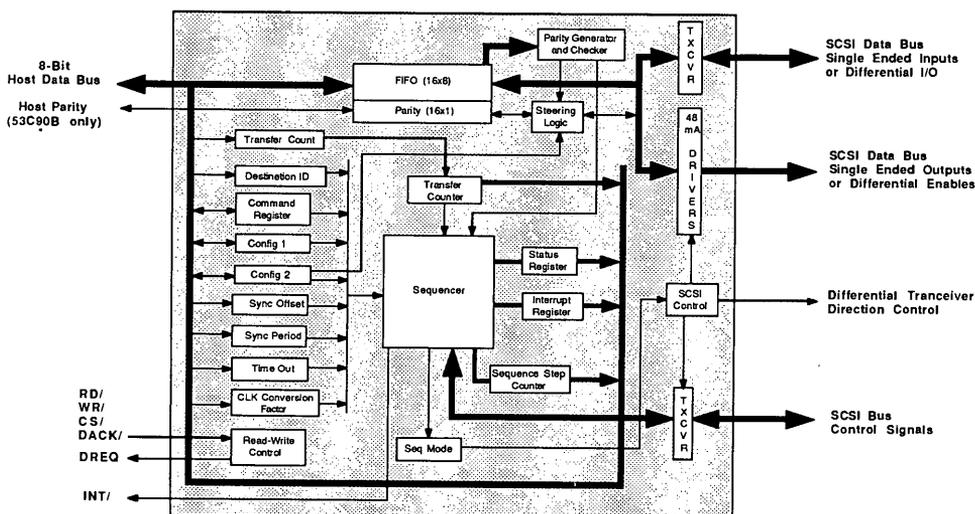# 53C90A and 53C90B
Advanced SCSI Controller

- ANSI X3.131-1986 Compatible
- On-chip 48 mA drivers
- Control logic for Differential Tranceivers
- Parity Generation , optional Checking
- Parity Pass-Thru (53C90B only)
- Programmable Transfer Period
- Programmable Offset
- SCSI-2 Tagged Queuing

- 16-byte FIFO
- 12 MegaByte/second DMA interface
- up to 5 MB/S Asynchronous SCSI
- up to 5 MB/S Synchronous SCSI
- 25 MHz clock
- Low Power CMOS
- 68 pin PLCC and 80 pin QFP

The 53C90A and 53C90B are high performance CMOS devices conforming to the ANSI standard, X3.131-1986, for Small Computer Systems Interface. They are a super-set of the 53C90 with additional commands and a second configuration register. The C90A is intended to directly replace a C90 in an existing design, allowing an easy upgrade to SCSI-2. The C90B has a parity pin on the host processor interface, but is otherwise identical to the C90A. Both are 100% compatible with existing 53C90 software.

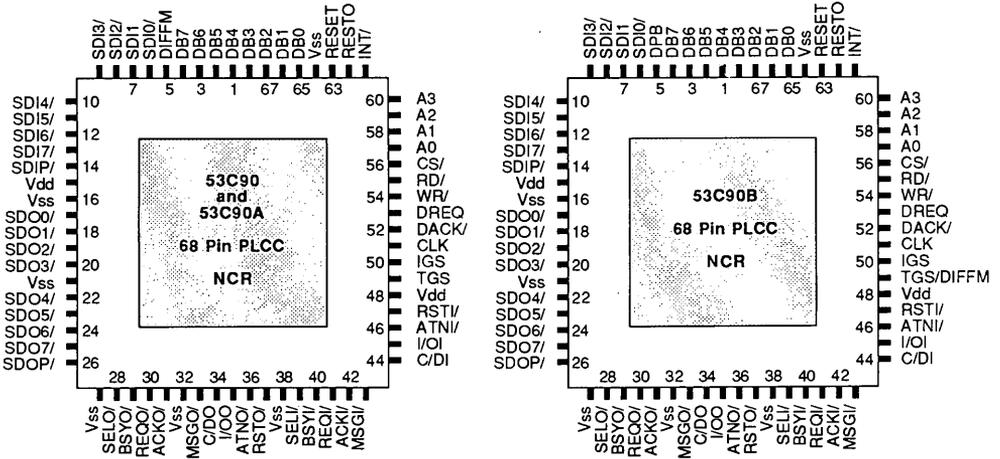The C90 Family reduces protocol overhead by performing common SCSI algorithms, or sequences, in response to a single C90 command. The C90A and C90B will operate at sustained data transfer rates of 5 MegaBytes per second in synchronous mode and 5 MegaBytes per second in asynchronous mode. See the section *Data Transfer Rate*.
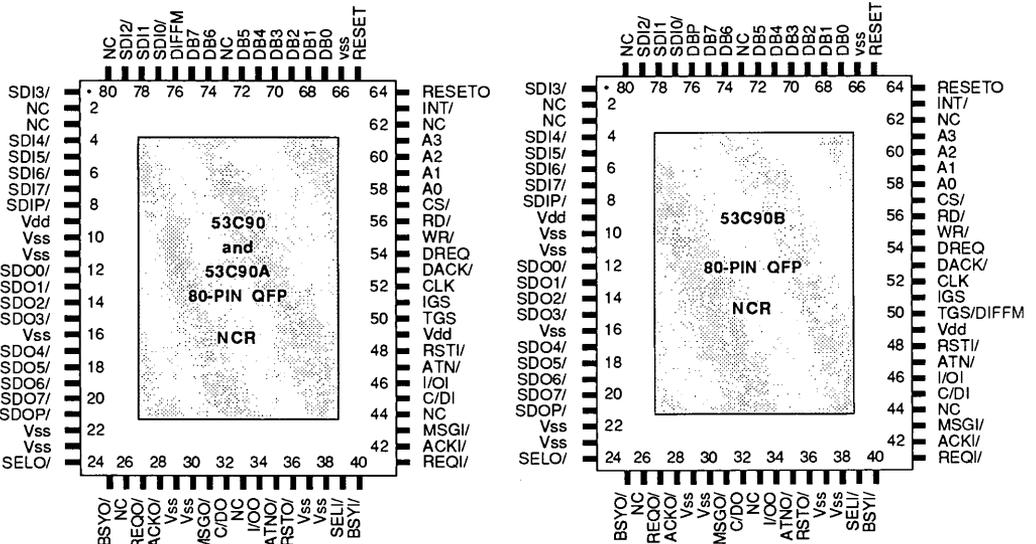

53C90A and 53C90B Block Diagram
Figure 1

1

PLCC Pin Diagram
Figure 2

QFP Pin Diagram
Figure 3

2

Host Processor and DMA Interface			
Pin #	Type	Signal	Description
4-1, 68-65	B	DB7-DB0	Active-high data bus connected to the DMA Controller, CPU and buffer memory. Each pad contains a pull-up to Vdd (12.5K minimum).
63	I	RESET	Active-high chip reset. Reset must be asserted for two CLK periods, mimimum, after the voltage on the power pins has reached VDD min. This input must not be connected to RESETO.
62	O	RESETO	Active-high reset output. This output is always asserted when the RESET input is true OR may be asserted when the SCSI Reset signal is active if bit 6 of the CONFIG-1 register is cleared AND the host has not serviced the interrupt (generated because of SCSI Reset) within 1-2 mS (depending on CLK frequency and Clock Conversion Factor--see Bus Initiated Reset).
61	O	INT/	Active-low, open drain interrupt signal to the microprocessor. It is latched on the rising edge of CLK and may be cleared by reading the Interrupt Register or by a host hardware RESET or by a host software reset (but not by a SCSI Reset). This output cannot be disabled internally.
60-57	I	A3-A0	Active-high address bus which specifies one of the ASP's internal registers for reading or writing. Used with CS/, ignored with DACK/.
56	I	CS/	Active-low chip-select signal which enables access to the ASP's internal registers. CS/ accesses any register--including the FIFO--while DACK/ accesses only the FIFO. CS/ and DACK/ must never be active at the same time.
55	I	RD/	Active-low read signal which enables ASP data onto DB7-DB0. CS/ or DACK/ must also be active.
54	I	WR/	Active-low write signal which strobes DB7-DB0 data into the ASP. CS/ or DACK/ must also be active.
53	O	DREQ	TriState active-high DMA request to the DMA Controller. DREQ will be true as long as the FIFO has at least one byte to send to memory, or has room to receive at least one byte from memory, depending on data direction.
52	I	DACK/	Active-low DMA acknowledge from the DMA controller. DACK/ accesses the FIFO only, while CS/ accesses any register--including the FIFO. CS/ and DACK/ must never be active at the same time. DACK/ must toggle true then false for every byte transfered. See DREQ Hi-Z bit in Config2.
51	I	CLK	Square wave clock which generates internal chip timing. The maximum frequency is 25 MHz, with a 35% to 65% duty cycle. The minimum frequency required for asynchronous SCSI transmission is 10 MHz. The minimum frequency required for synchronous transmission is 12 MHz. The synchronous transmission rate is equal to the CLK input period divided by the value in the Synchronous Transfer Period Register. The asynchronous transfer rate is indirectly affected by CLK frequency. See section Data Transfer Rate

Host Processor and DMA Interface Pins (PLCC Package)
Table 1

SCSI Bus Interface			
Pin #	Type	Signal	Description
6-13 14	B	SDI0/-SDI7/ SDIP/	Schmitt trigger, active-low SCSI data/parity bus. In single-ended mode (DIFFM=0), these inputs are SCSI Data bus signals. In differential mode (DIFFM=1), these are bi-directional data and parity signals for external SCSI bus transceivers.
17-20 22-25 26	O O	SDO0/-SDO7/ SDOP/	48 mA, open drain SCSI data/parity bus. In single-ended mode (DIFFM=0), these outputs are active-low SCSI data signals. In differential mode (DIFFM=1), these outputs are used to control the direction of external differential transceivers; with high meaning output to the SCSI bus, low meaning input from the SCSI bus.
28	O	SELO/	48 mA, open drain SCSI Select signal. In single-ended mode, this output is active low. In differential mode, it is active high.
29	O	BSYO/	48 mA, open drain SCSI Busy signal. In single-ended mode, this output is active low. In differential mode, it is active high.
30	O	REQO/	48 mA, open drain, active-low SCSI Request signal. This output is only asserted when the ASP is in Target mode.
31	O	ACKO/	48 mA, open drain, active-low SCSI Acknowledge signal. This output is only asserted when the ASP is in Initiator mode.
33-35	O	MSGO/, C/DO, I/OO	48 mA, open drain, active-low SCSI phase signals. These outputs are only asserted when the ASP is in Target mode.
36	O	ATNO/	48 mA, open drain, active-low SCSI Attention signal. This output is only asserted when the ASP is in Initiator mode. Several ASP commands will set ATN. It is also asserted when the ASP detects an incoming parity error if parity checking is enabled.
37	O	RSTO/	48 mA, open drain SCSI Reset signal. In single-ended mode, this output is active low. In differential mode, it is active high. The ASP drives this signal true only when the host writes the SCSI Bus Reset command to the command register. The pulse length is 25-40 μS, depending on CLK frequency and Clock Conversion Factor. See Bus Initiated Reset.
39	I	SELI/	Schmitt trigger, active-low SCSI Select input.
40	I	BSYI/	Schmitt trigger, active-low SCSI Busy input.
41	I	REQI/	Schmitt trigger, active-low SCSI Request input.
42	I	ACKI/	Schmitt trigger, active-low SCSI Acknowledge input.
43	I	MSGI/	Schmitt trigger, active-low SCSI Message input.
44	I	C/DI	Schmitt trigger SCSI Control/Data input.

SCSI Bus Pins (PLCC Package)
Table 2

SCSI Bus Interface (continued)			
Pin #	Type	Signal	Description
45	I	I/OI	Schmitt trigger SCSI Input/Output input.
46	I	ATNI/	Schmitt trigger, active-low SCSI Attention input.
47	I	RSTI/	Schmitt trigger, active-low SCSI Reset signal. When this input is true, the ASP will automatically disconnect from the SCSI bus. If bit 6 in the CONFIG-1 register is zero, the ASP will interrupt the host. If the interrupt is not serviced within 1-2 mS, the ASP will reset its host processor. See the section Bus Initiated Reset.
50	O	IGS	Active-high initiator group select signal. This pin is high whenever the ASP is in initiator mode. It is used in differential mode to enable the initiator signals (ACKO/, ATNO/). When low the ASP should be receiving these signals.

SCSI Bus Pins (PLCC package)
Table 2 (continued)

Power and Ground Pins			
PLCC Pin Number	QFP Pin Number	Label	Description
15, 48	9, 49	Vdd	+5 Volt Power input.
16, 21, 27 32, 38, 64	10, 11, 16 22, 23, 29 30, 37, 66	Vss	Ground. NCR recommends a ground plane be used.

Power and Ground Pins
Table 3

53C90 and 53C90A only			
Pin #	Type	Signal	Description
49	O	TGS	Active-high Target Group Select signal. This pin is high whenever the ASP is in target mode. It is used in differential mode to enable the target signals (REQO/, MSGO/, C/DO, I/OO). When low, the ASP should be receiving these signals.
5	I	DIFFM	Differential mode enable. When this pin is grounded the ASP operates in single-ended mode, with separate SCSI data input and output buses. When this pin is high the ASP operates in differential mode, with bidirectional SCSI data on the SDI pins and active-high differential transceiver enables on the SDO pins.

Pins Unique to 53C90 and 53C90A (PLCC Package)
Table 4

53C90B only			
Pin #	Type	Signal	Description
49	B	TGS/DIFFM	This pin is sampled during reset to put the chip in Differential Mode or Single-Ended Mode. It then switches function to become the TGS output. An internal pull-up pulls it high for single-ended mode; an external 1k pull-down will place the C90B in differential mode.
			There two kinds of reset: Power-Up Reset, and Running-Reset. On power-up, the state of this pin is sampled as the voltage on the power pins rises through 3 volts (approximately). A running-reset is a host hardware reset that occurs sometime later. A running-reset will sample this pin until the 10th rising edge of CLK after RESET goes true (high). This is enough time for the internal pull-up to pull it high. Whatever state it's in on the 10th clock will determine the mode. The TGS function will be disabled until the12th rising edge of CLK after RESET first goes true and RESET is false.
			When RESET is false (low), and 12 clocks have occured since RESET first went true, this pin becomes the TGS output; an active-high Target Group Select signal. This pin is high whenever the ASP is in target mode. It is used in differential mode to enable the target signals (REQO/, MSGO/, CDO/, IOO/). When low the ASP should be receiving these signals.
5	B	DBP	Active high Data Bus Parity for host, DMA, and memory data bus. Four bits in Config-1 and Config-2 control parity generation and checking.

Pins Unique to the 53C90B (PLCC Package)
Table 5

DIFFERENCES FROM 53C90

- supports three byte message exchange in SCSI-2 tagged queuing
- added Select with ATN3 command
- added Target DMA Abort command
- added interrupt polling bit
- added second configuration register
- improved immunity to cable impedance mismatches and improper termination
- Tri-State DMA Request output
- cut leakage current on SCSI input pins when powered off
- relaxed register timings
- relaxed DMA timings
- relaxed CLK duty cycle
- lengthened Read Data Access time
- NOP required less often

FUNCTIONAL DESCRIPTION

The ASC SCSI Data Bus has a set of inputs and a set of outputs. This allows the ASC to be used in either single-ended mode or differential mode. In single-ended mode, the inputs are usually connected to the outputs on the circuit board. In differential mode, the SDI (SCSI Data Input) pins become bi-directional data pins, while the SDO (SCSI Data Output) pins become enable signals for the differential transceivers. Separate enables are required because, during Arbitration, two data bus signals must be outputs while the other six must be inputs. Two signals, TGS and IGS, control the direction of the external transceivers--allowing the ASC to dynamically switch between Initiator and Target roles.

The ASC has a command set that allows it to perform common SCSI sequences at hardware speed without host intervention. Its on-chip FIFO may be accessed simultaneously by the SCSI bus and either the host processor or the host DMA controller. All Command, Data, Status and Message bytes pass through the FIFO on their way to or from the SCSI bus. Most ASC commands have two versions: DMA and non-DMA. When DMA instructions are used, data will pass between memory and the SCSI bus with the FIFO acting as temporary storage when the DMA channel is temporarily shut down by a higher priority event, such as DRAM refresh.

The FIFO also helps speed execution during non-DMA transfers. For example, in Initiator role, the host processor will load the Command Descriptor Block and optionally, one or three Message bytes into the FIFO, issue one of several Selection commands and wait for an interrupt. The ASC will wait for Bus Free; Arbitrate for the bus--again and again until it acquires it; send the Message bytes, followed by the Command Descriptor Block; then generate an Interrupt. Meanwhile, a multi-tasking host may continue with other tasks.

In Target role, the host processor will Enable Selection, then wait for an interrupt. Eventually, an Initiator will select the ASC. It will then automatically step through the Arbitration Phase, Selection Phase and Command Phase before generating an interrupt. When the interrupt occurs, the entire Command Descriptor Block will be in the FIFO along with any Message bytes sent by the Initiator. Combination commands, such as these, are identified with the *sequence* suffix in the table of ASC commands.

After Selection Phase has been successfully completed, the ASC may transfer bytes in any of the SCSI Information Phases whether operating in Initiator or a Target role. The ASC supports Disconnect-ReSelect in both Initiator and Target roles-- making high performance multi-threaded systems easy to implement.

The ASC may transfer Data Phase bytes across the bus synchronously, at speeds up to 5 MB/s, or asynchronously at speeds up to 6 MB/s. See the section *Data Transfer Rate*. The difference between the two is transparent to the user except that the Synchronous Offset and the Synchronous Transfer Period registers must be programmed prior to synchronous data trans-

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fer. The default, after hardware or software reset, is asynchronous transmission. Data Phase bytes will usually be transferred using DMA. The host processor will program an external DMA controller, program the ASC Transfer Count, issue an ASC data transfer command (there are several), then wait for an interrupt. The DMA controller and the ASC will transfer all the data without host processor intervention.

To end the SCSI transaction, the ASC Target will place a Status byte and a Message byte in the FIFO; then issue a single command (there are two to chose from) which will cause the ASC to first assert Status Phase, send the first byte, assert Message In Phase, send the second byte, disconnect from the SCSI bus (after the Initiator releases ACKnowledge) and interrupt the host processor.

The end of a SCSI transaction is similar for an ASC Initiator except that it receives two bytes into its FIFO. The Initiator prevents the Target from disconnecting by holding ACKnowledge asserted on the bus while the host processor examines the Status and Message bytes. If both bytes are good, the Message Accepted command is used to instruct the ASC to release ACK, which allows the Target to disconnect which causes the Initiator to interrupt its host and report the disconnect. If the Status and Message bytes are not good, the host should first issue the Set ATN command before issuing the Message Accepted command. This instructs the ASC to assert ATN (Attention) before releasing ACK, which should cause the Target to request Message Out Phase rather than disconnect.

BUS INITIATED SEQUENCES

• Selection
• ReSelection
• SCSI Bus Reset

Selection or ReSelection sequences occur in the disconnected state when the ASC is Selected or ReSelected by another Initiator

or Target--if the Enable Selection or ReSelection Command had previously been received by the ASC.

In addition to responding to bus initiated events, the ASC may initiate a bus event by using one of several Selection or ReSelection Commands. If one of these commands starts executing, **it will clear Enable Selection/ReSelection** after Arbitration has been won. Normally the host processor will have 250 mS (ANSI recommended Selection Time-Out period) after the chip disconnects from the bus to re-enable bus initiated events. If the time-out is exceeded, an Initiator or Target which is attempting to connect to the ASC, may timeout and abort.

If, on the other hand, the bus initiated event occurs before the command starts executing, the FIFO will be cleared, the Command Register will be cleared, and any further writes by the host processor will be ignored until the Interrupt Register is read. Since a Selection or ReSelection command requires that something be placed in the FIFO, these bytes will be lost--as will any command written to the Command Register. The interrupt handler that services a Selection or ReSelection command will have to examine the bits in the Interrupt register to determine if the ASC Selected another device, or if it was Selected by another device. The former case will cause a Function Complete interrupt, the latter case will cause a Selection or ReSelection interrupt.

Bus Initiated Selection

When the ASC has been Selected as a Target, the following data will be in its FIFO:

- Bus ID
- Identify Message
- Command Descriptor Block

The Bus ID will always be present and will always be one byte. It is an un-encoded version of the state of the bus during Selection Phase. Any SCSI data bits that

were true during Selection Phase will be set. The Target ID (our ID) must always be set. In Arbitrating systems, the Initiator ID must also be set. The Initiator ID is optional in non-arbitrating systems.

The Identify Message will always be present in the FIFO and will always be one byte in SCSI-1 systems but may be one or three bytes in SCSI-2 systems. If the Initiator does not send an Identify Message (does not Select with ATN), a null byte (00h) will be placed in the FIFO.

If the Initiator Selects with ATN and the SCSI-2 bit is cleared, the ASC Target will request one Message byte and will place it in the FIFO behind the Bus ID. The ASC will then begin requesting Command Phase bytes unless the Message byte is not a valid Identify Message, or a parity error is detected--which will cause the ASC to interrupt and stop. The Sequence Step Register should then be examined.

If the Initiator Selects with ATN and the SCSI-2 bit is set, the ASC will examine both the Message byte and the ATN signal to determine how many bytes to request. If the first byte is a valid Identify Message and if ATN goes false after receiving the first byte, the ASC will only request one message byte. If the first byte is a valid Identify Message byte and ATN is still true, it will request two more Message bytes. The ASC will then begin requesting Command Phase bytes unless the first byte was not a valid Identify Message, or a parity error was detected, or ATN went false between the 2nd and 3rd bytes, or ATN remained true but the SCSI-2 bit was false; which will cause the ASC to interrupt and stop. The Sequence Step Register should then be examined.

The Command Descriptor Block (CDB) will be placed in the FIFO behind the message byte(s), assuming Selection completed normally. The CDB may be 6, 10 or 12 bytes long. Thus, in SCSI-2, the entire FIFO may be filled if a tagged queue twelve byte command is used.

Bus Initiated ReSelection

The ASC will allow itself to be ReSelected as an Initiator by a Target if it has previously received the Enable Selection-ReSelection command. If the sequence completes normally, the following information will be in the FIFO:

- Bus ID
- Identify Message

The Bus ID is the same as the Selection case, described above. The Identify message will always be present and always be one byte.

Bus Initiated Reset

A bus initiated reset will be recognized by the ASC at any time. The ASC will then disconnect from the bus and reset its internal sequencer. If the SCSI Reset Reporting bit (Configuration-1 Register) is not set the ASC will generate a SCSI Reset Detected interrupt. If the host processor does not read the Interrupt Register within T1 milliseconds, the ASC will assert RESETO for T2 microseconds.
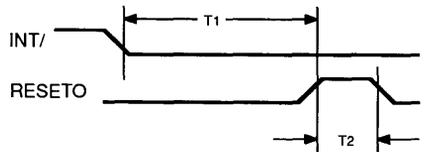
Interrupt and Reset Timing
Figure 4

$T1 = 2(CLK\ period)[3841CCF - 1]$
$T2 = 130(CLK\ period)(CCF)$

where CCF=Clock Conversion Factor (see description of write register 09).

For example, at CLK= 25 MHz
$T1 = 1.5\ mS$
$T2 = 26\ \mu S$

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DATA TRANSFER RATE

Performance claims for the ASC are based on it being directly connected to the SCSI bus with no external transceivers. In differential mode, external transceivers are required and will slow asynchronous transmission by the propagation delay of the chosen transceiver but will not slow synchronous transmission.

The synchronous data transmission rate is equal to the CLK input frequency divided by the encoded value in the Synchronous Period Register. Sustained synchronous transfer rates of 5 MegaBytes per second are attainable across the commercial voltage and temperature range.

The asynchronous transmission rate will vary with cable length and the CLK period. The ASC can reach sustained transfer rates of 6 Megabytes per second on short (one foot) cables using typical devices operating at or near nominal voltage and temperature. The worst case asynchronous transmission rate, over voltage, temperature, and process variations is 3 MB/s on a maximum length (single-ended) cable and 4.5 MB/s on a one foot cable.

The asynchronous transmission rate is only slightly affected by the CLK frequency when sending data; the ASC will drive the data bus for a minimum of one CLK period before asserting REQ or ACK. The CLK frequency does not affect the asynchronous transfer rate when receiving data.

REGISTER SET		
Address (hex)	Read	Write
0	Transfer Counter LSB	Transfer Count LSB
1	Transfer Counter MSB	Transfer Count MSB
2	FIFO	FIFO
3	Command	Command
4	Status	Destination Bus ID
5	Interrupt	Select/Reselect Timeout
6	Sequence step	Synchronous Period
7	FIFO Flags/Sequence Step	Synchronous Offset
8	Configuration 1	Configuration 1
9	NCR Reserved	Clock Conversion Factor
A	NCR Reserved	Test Mode
B	Configuration 2	Configuration 2

ASC Register Set
Table 6

REGISTER SET

Some ASC registers have a different meaning during read than write. When CS/ is true, the register being accessed is determined by either RD/ or WR/ together with the address pins A0-3. The FIFO may be accessed using either CS/ or DACK/ together with RD/ or WR/. Address pins A0-A3 are ignored when DACK/ is active, but must be driven when CS/ is active.

Transfer Count   Write Address 0,1

These two registers together form a 16-bit Transfer Count for DMA operations. It specifies the number of bytes that are to be transferred over the SCSI bus. Values written to these two registers will be stored internally and loaded into the Transfer Counter by any DMA command. These values remain unchanged while the transfer counter decrements. Thus, successive

blocks of equal size may be transferred without reprogramming the count. They may be reprogrammed any time after the previous DMA operation has started-- whether it has finished or not. Zero specifies a maximum length count (65536). These registers are not changed by any reset; their states are unpredictable after power-up.

Transfer Counter   Read Address 0,1

A read from these two addresses will return the value currently in the counter. DMA commands use the counter to terminate a transfer. Any DMA command will load Count into the Counter. A DMA NOP (80 hex) will load the counter while the non-DMA NOP (00) will not.

With one exception, non-DMA commands do not use the counter. The exception is when the ASC has been Selected. It decodes the Group Code field of the Command Descriptor Block, loads the Counter with the number of bytes in the CDB, then decrements once for every byte received.

The transfer counter decrements on the leading edge of:

Target	Decremented by
Data In Phase	DACK/
Data Out Phase	REQO/

Initiator	Decremented by
Synchronous Data In	DACK/
Asynchronous Data In	ACKO/
Data Out	DACK/

Note that DACK/ can decrement the counter even if RD/ or WR/ do not go true. False DACK's can cause the counter to get out of sync with the data stream--leading to subtle errors that are difficult to trace. When false DACK's are expected to interfere with a temporarily suspended DMA operation, the DREQ Hi-Z bit in Config-2 should be set.

FIFO Register   Read/Write Address 02

The FIFO is a 16 by 9 bit First In First Out buffer between the SCSI bus and memory. It is accessible by the host processor at this address. It is also accessible by an external DMA controller and by the SCSI bus. The DMA may access the FIFO by asserting DACK/ together with either RD/ or WR/. When accessed by CS/, the address bits must be valid. When accessed by DACK/, the address bits are ignored. The bottom FIFO element and the FIFO Flags are initialized to zero during hardware RESET, software Reset Chip and at the beginning of Bus Initiated Selection or ReSelection. The contents of the rest of the FIFO are not changed by any reset, but when the flags are zero, successive FIFO reads will always access the bottom register.

Command Register   R/W Address 03

The Command Register is a two-deep eight-bit read/write register used to give commands to the ASC. Up to two commands may be stacked in the Command Register. The second command may be written before the ASC completes (or even starts) the first. Reset Chip, Reset SCSI Bus and Target Stop DMA execute immediately; all others wait for the previous command to complete. The last executed (or executing) command will remain in the Command Register and may be read by the host processor. Reading the Command Register has no effect on its contents. The Command Register will be cleared by any of the following conditions:

• Hardware, Software or SCSI bus Reset
• SCSI bus Disconnect
• Bus-initiated Selection or ReSelection
• Select Command
• Reconnect Command if ATN is set
• Select or ReSelect Time-out
• Target Terminate Command
• Parity Error detected in Target Mode
• Assertion of ATN in Target Mode
• Any phase change in Initiator Mode
• Illegal Command

If two commands are placed in the Comand
Register, two interrupts may result. If the
first interrupt is not serviced before the
second finishes, the second interrupt is
stacked behind the first. When the Inter-
rupt Register is read by the host to service
the first interrupt, the contents Status Reg-
ister, Sequence Step Register, and Interrupt
Register will change to describe the second
interrupt.

Command Register

DMA			Command			
7	6	5	4	3	2	1	0
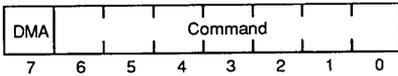
Read-Write Address 03
Figure 5

Bit 7   Enable DMA

When bit 7 is not set, the command is a
non-DMA instruction. When it is set, the
command is a DMA instruction. DMA in-
structions will load the internal byte-counter
with the value in the Transfer Count Reg-
ister (without changing the Count Register)
then transfer data until that count decre-
ments to zero. If the transfer terminates
prematurely, the bits in the Status Register,
Sequence Step Register and Interrupt Reg-
ister will indicate why.

Bits 6-0   Command Code

The ASC commands are shown in table 19.
Bits 4, 5 and 6 specify a mode group.
Commands from the Miscellaneous group
may be issued at any time. Commands
from the Disconnected, Target or Initiator
groups will only be accepted by the ASC if
it is in the same mode as the command
when that command falls to the bottom of
the Command FIFO. Otherwise, an Illegal
Command Interrupt will be generated. For
example, after hardware or software reset,
the ASC will be in the Disconnected state.
A command from either the Target group or
the Initiator group will cause an Illegal
Command interrupt. An Enable

Selection/ReSelection command by itself
will not change modes. However, if an-
other SCSI device then Selects the ASC, it
will be in the Target state; if another device
ReSelects the ASC, it will then be in the
Initiator State. Similarly, any Select com-
mand will place the ASC in Initiator mode,
while the ReSelect Sequence command will
place the ASC in Target mode.

Status Register   Read Address 04

The Status Register contains important
flags that indicate various conditions. All
but the phase bits are latched. The phase
bits are live indicators of the state of the
SCSI bus. All the latched bits except the
Terminal Count are cleared by reading the
Interrupt Register.

Status Register Read Address 04

INT	GE	PE	TC	VGC	MSG	C/D	I/O
7	6	5	4	3	2	1	0
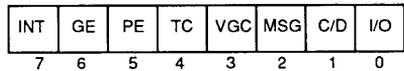
Bits 2 1 0	SCSI Phase
0 0 0	Data Out
0 0 1	Data In
0 1 0	Command
0 1 1	Status
1 0 0	ANSI Reserved
1 0 1	ANSI Reserved
1 1 0	Message Out
1 1 1	Message In

Figure 6

Bit 7   Interrupt

This bit is set whenever the ASC is driving
the INT output true. It may be polled. It is
buffered from the actual output, so that in
wired-OR (shared interrupt) designs, this
bit will indicate whether the ASC is at-
tempting to interrupt the host processor.
This bit was reserved by NCR in the

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53C90. Hardware RESET or software Reset Chip or a read from the Interrupt Register will release an active INT signal and also clear this bit.

Bit 6   Gross Error

This bit is set when one of the following has occurred:

1) The top of the FIFO has been overwritten
2) The top of the Command Register has been overwritten
3) Direction of DMA transfer is opposite the direction of SCSI transfer
4) Unexpected phase change in Initiator role during synchronous Data Phase

Gross Error does not cause an interrupt; it may be detected only while servicing another interrupt. The bit is cleared by reading the Status Register if the interrupt output is asserted. It will also be cleared by hardware RESET, or software Reset Chip (but not SCSI reset).

Bit 5   Parity Error

This bit will be set if parity checking is enabled in the Config-1 Register and the ASC detects a SCSI parity error on incoming Command, Data, Status or Message bytes. It will be cleared by reading the Interrupt Register if the interrupt output is asserted. Hardware RESET or software Reset Chip will clear this bit (but not SCSI reset).

Bit 4   Terminal Count

This bit is set when when the Transfer Counter decrements to zero. It resets when the Transfer count is loaded. Since a DMA NOP (80 hex) command will load the Transfer Counter, it will also clear this bit. Note that a non-DMA NOP (00) will not load the counter and will not clear this bit. Reading the Interrupt register will not clear this bit. Hardware RESET or software

Reset Chip will clear it (but not SCSI reset).

Bit 3   Valid Group Code

The name of this bit has changed from Transfer Complete in the 53C90 to Valid Group Code in the 53C90A and 53C90B; but its function remains the same.

When the ASC is Selected, it decodes the Group Code field in the first byte of the Command Descriptor Block. If the Group Code matches one defined in X3.131-1986, this bit will be set. An undefined Group Code (designated *reserved* by the ANSI committee) leaves it not set. If the SCSI-2 bit is set in the Config-2 register, Group 2 commands will be recognized as ten byte commands and the bit will be set. If the SCSI-2 bit is cleared, Group 2 commands will be treated as reserved commands. Groups 3 and 4 are always treated as reserved commands. A reserved group command will cause the ASC to request 6 command bytes. The ASC recognizes Group 6 as six-byte vendor unique commands and Group 7 as ten-byte vendor unique commands. The Valid Group Code bit will be cleared by reading the Interrupt Register if the interrupt output is asserted. It will also be cleared by hardware RESET or software Reset Chip (but not by SCSI reset).

Bits 2-0   Phase Bits

These bits indicate the phase on the SCSI bus at the time the register was read. These bits are live; if the phase changes, so will these bits. In Target role, the ASC is driving these lines so they will not change if the read follows an interrupt. In Initiator role, the ASC will generate its interrupt only after the Target asserts REQuest. The ANSI specification requires that the phase lines be valid before asserting REQuest and remain valid until the Initiator asserts ACKnowledge. Thus, these bits can be expected to be stable during any read that follows an interrupt.

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Destination ID   Write Address 04

The least significant 3 bits of this register
specify the encoded destination bus ID for a
Selection or ReSelection command. These
bits are binary encoded, with 111 repre-
senting device ID 7 which appears as 80
hex on the SCSI bus. The most significant
5 bits are reserved by NCR. The Destina-
tion ID is not changed by any reset; the
states of these bits are unpredictable after
power-up.

Interrupt Register   Read Address 05

This 8-bit register is used in conjunction
with the Status Register and Sequence Step
Register to determine the cause of an inter-
rupt. Reading this register when the inter-
rupt output is true will clear all three regis-
ters. The entire Interrupt Register will be
cleared (0) by hardware RESET or soft-
ware Reset Chip (but not SCSI reset).

Interrupt Register

SCSI RST	Ill CMD	Dis	BS	FC	Re SEL	SEL ATN	SEL
7	6	5	4	3	2	1	0

Read Address 05
Figure 7

Bit 7   SCSI Reset Detected

This bit is set if the SCSI Reset Reporting
bit in the Config-1 Register is set to zero
and the chip detects a reset on the SCSI
bus. If the interrupt is not serviced in one
or two milliseconds (refer to Bus *Initiated
Reset*) the ASC resets the host.

Bit 6   Illegal Command

This bit is set when an unused code is
placed in the Command Register or when
the command is from a mode group differ-
ent than the mode the ASC is currently in.
Refer to the definition of the Command
Register.

Bit 5   Disconnect

In Initiator mode, this bit is set when the
Target disconnects or a Selection or ReSe-
lection Time-out occurs. When the ASC is
in Target mode, this bit is set when a
Terminate Sequence, or Command Com-
plete Sequence command causes the ASC
to disconnect from the bus.

Bit 4   Bus Service

This bit indicates that the other device is re-
questing service. In Target mode, it is set
whenever the Initiator asserts Attention
(ATN). In Initiator mode, it is set when-
ever the Target is requesting an Information
Transfer Phase.

Bit 3   Function Complete

This bit will be set after any Target mode
command has completed. In Initiator
mode, it is set after a Target has been se-
lected (before transferring any Command
Phase bytes), after Command Complete
finishes, or after a Transfer Info command
when the Target is requesting Message In
Phase.

Bit 2   ReSelected

This bit is set during ReSelection Phase to
indicate that the ASC has been ReSelected
as an Initiator.

Bit 1   Selected with ATN

This bit is set during Selection Phase to in-
dicate that the ASC has been Selected as a
Target and that ATN (Attention) was as-
serted on the SCSI bus.

Bit 0   Selected

This bit is set during Selection Phase to in-
dicate that the ASC has been Selected as a

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Target and that ATN (Attention) was false during Selection.

Time-Out   Write Address 05

This 8-bit write-only register specifies the amount of time to wait for a response during Selection or ReSelection. (The ASC has no way to time-out if it never wins Arbitration--it will keep trying indefinitely until it wins). The Time-Out Register is normally loaded to specify a time-out period of 250 milliseconds. The register value (RV) may be calculated from:

$$RV = \frac{(Time\text{-}out\ Period)(CLK\ Frequency)}{8192(Clock\ Conversion\ Factor)}$$

For example, at 25 MHz, the register value that gives a 250 mS time-out period is 153 decimal or 99 hexadecimal. The Clock Conversion Factor is defined in the description of Write Address 9. The Time-Out Register remains unchanged by any reset; the states of these bits are unpredictable after power-up.

Synchronous Transfer Period
                         Write Address 6

The lower five bits of this register specify the minimum time between leading edges of successive REQuest or ACKnowledge pulses. Synchronous data will be trans-mitted or received at the rate of one byte every N clocks (CLK). N is related to the register value as shown below.

Register Value	clocks per byte
0 0 1 0 0	5
0 0 1 0 1	5
0 0 1 1 0	6
0 0 1 1 1	7
•	•
•	•
•	•
1 1 1 1 1	31
0 0 0 0 0	32
0 0 0 0 1	33
0 0 0 1 0	34
0 0 0 1 1	35

Missing entries, in the table above, follow the Binary Code. The upper three bits are reserved by NCR. This register defaults to 5 after hardware RESET or software Reset Chip (but not SCSI reset).

Sequence Step   Read Address 06

The lower 3 bits of this register are used to indicate how far the internal sequencer was able to proceed in executing combination commands. This counter will be incremented at certain points in various algorithms to aid in error recovery if the previous command does not complete normally.

Initiator Select with ATN and Stop		
Sequence Step 2 1 0	Interrupt Register 7 6 5 4 3 2 1 0	Interpretation
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; Selection Time-Out; disconnected
0 0 0	0 0 0 1 1 0 0 0	Arbitration and Selecton Complete. Stopped because Target did not assert Message Out Phase. ATN still asserted by ASC.
0 0 1	0 0 0 1 1 0 0 0	Message Out Complete. Sent one Message Byte; ATN on.

Sequence Step
Table 7

Initiator Select without ATN		
Sequence Step 2 1 0	**Interrupt Register** 7 6 5 4 3 2 1 0	**Interpretation**
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; Selection Time-Out; disconnected
0 1 0	0 0 0 1 1 0 0 0	Arbitration and Selection Complete. Stopped because Target did not assert Command Phase.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer because Target prematurely changed phase.
1 0 0	0 0 0 1 1 0 0 0	Select sequence complete.

Sequence Step
Table 8

Initiator Select with ATN		
Sequence Step 2 1 0	**Interrupt Register** 7 6 5 4 3 2 1 0	**Interpretation**
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; Selection Time-Out; disconnected
0 0 0	0 0 0 1 1 0 0 0	Arbitration and Selection Complete. Stopped because Target did not assert Message Out Phase. ATN still still driven by ASC.
0 1 0	0 0 0 1 1 0 0 0	Message Out Complete. Sent one Message Byte with ATN true, then released ATN. Stopped because Target did not assert Command Phase after Message byte was sent.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change. Some CDB bytes may not have been sent; check FIFO Flags.
1 0 0	0 0 0 1 1 0 0 0	Selection with ATN sequence complete.

Sequence Step
Table 9

Initiator Select with ATN3		
Sequence Step 2 1 0	Interrupt Register 7 6 5 4 3 2 1 0	Interpretation
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; Selection Time-Out; disconnected
0 0 0	0 0 0 1 1 0 0 0	Arbitration and Selection Complete. Stopped because Target did not assert Message Out Phase. ATN still still driven by ASC.
0 1 0	0 0 0 1 1 0 0 0	Sent 1, 2 or 3 Message Bytes. Stopped because Target prematurely changed from Message Out Phase or did not assert Command Phase after 3rd Message byte. ATN released only if 3rd Message byte was sent.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change. Some CDB bytes may not have been sent; check FIFO Flags.
1 0 0	0 0 0 1 1 0 0 0	Selection with ATN3 sequence complete.

Sequence Step
Table 10

Target Selected without ATN		
Sequence Step 2 1 0	Interrupt Register 7 6 5 4 3 2 1 0	Interpretation
0 0 0	0 0 0 0 0 0 0 1	Selected, loaded Bus ID into FIFO, loaded null-byte message into FIFO.
0 0 1	0 0 0 0 0 0 0 1	Stopped in Command Phase due to parity error. Some Command Descriptor Block bytes may not have been received. Check FIFO Flags.
0 0 1	0 0 0 1 0 0 0 1	Same as above, Initiator asserted ATN in Command Phase.
0 1 0	0 0 0 0 0 0 0 1	Selected, received entire Command Descriptor Block. Check Valid Group Status bit.
0 1 0	0 0 0 1 0 0 0 1	Same as above, Initiator asserted ATN in Command Phase.

Sequence Step
Table 11

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Target Selected with ATN SCSI-2 bit not set		
Sequence Step 2 1 0	Interrupt Register 7 6 5 4 3 2 1 0	Interpretation
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN, stored Bus ID and one message byte. Stopped due either to Parity Error or invalid ID Message.
0 0 0	0 0 0 1 0 0 1 0	Selected with ATN, stored Bus ID and one Message byte. Stopped because ATN remained true after 1st Message byte.
0 0 1	0 0 0 0 0 0 1 0	Stopped in Command Phase due to Parity Error. Some CDB bytes not received. Check Valid Group Code bit and FIFO Flags.
0 0 1	0 0 0 1 0 0 1 0	Stopped in Command Phase. Parity Error and ATN true.
0 1 0	0 0 0 0 0 0 1 0	Selection Complete. Received one Message byte and the entire Command Descriptor Block.
0 1 0	0 0 0 1 0 0 1 0	Same as above, Initiator asserted ATN during Command Phase

Sequence Step
Table 12

Target Selected with ATN SCSI-2 bit set		
Sequence Step 2 1 0	Interrupt Register 7 6 5 4 3 2 1 0	Interpretation
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN, stored Bus ID and one message byte. Stopped due either to Parity Error or invalid ID Message.
1 0 0	0 0 0 0 0 0 1 0	Parity error during 2nd or 3rd Message byte.
1 0 0	0 0 0 1 0 0 1 0	ATN remained true after 3rd Message Byte.
1 0 1	0 0 0 0 0 0 1 0	Received 3 Message bytes then stopped in Command Phase due to Parity Error. Some CDB bytes not received. Check Valid Group Code bit and FIFO Flags.
1 0 1	0 0 0 1 0 0 1 0	Stopped in Command Phase. Parity Error and ATN true.
1 1 0	0 0 0 0 0 0 1 0	Selection Complete. Received 3 Message bytes and the entire Command Descriptor Block.

Sequence Step
Table 13

Target Receive Command		
Sequence Step 2 1 0	Interrupt Register 7 6 5 4 3 2 1 0	Interpretation
0 0 1	0 0 0 0 1 0 0 0	Stopped during command transfer due to parity error. Check FIFO Flags.
0 0 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to parity error. ATN asserted by Initiator.
0 1 0	0 0 0 0 1 0 0 0	Received entire Command Descriptor Block.
0 1 0	0 0 0 1 1 0 0 0	Received entire CDB, Initiator asserted ATN.

Sequence Step
Table 14

Target Disconnect Sequence		
Sequence Step 2 1 0	Interrupt Register 7 6 5 4 3 2 1 0	Interpretation
0 0 0	0 0 0 1 1 0 0 0	Sent one Message byte. Stopped because Initiator set ATN.
0 0 1	0 0 0 1 1 0 0 0	Sent two Message bytes. Stopped because Initiator set ATN.
0 1 0	0 0 1 0 1 0 0 0	Disconnect sequence complete. Disconnected, bus is free.

Sequence Step
Table 15

Target Terminate Sequence		
Sequence Step 2 1 0	Interrupt Register 7 6 5 4 3 2 1 0	Interpretation
0 0 0	0 0 0 1 1 0 0 0	Sent status byte. Stopped because Initiator set ATN.
0 0 1	0 0 0 1 1 0 0 0	Sent Status and Message bytes. Stopped because Initiator set ATN.
0 1 0	0 0 1 0 1 0 0 0	Terminate sequence complete. Disconnected, bus is free.

Sequence Step
Table 16

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Target Command Complete Sequence		
Sequence Step 2 1 0	Interrupt Register 7 6 5 4 3 2 1 0	Interpretation
0 0 0	0 0 0 1 1 0 0 0	Sent status byte. Stopped because Initiator set ATN.
0 0 1	0 0 0 1 1 0 0 0	Sent Status and Message bytes. Stopped because Initiator set ATN.
0 1 0	0 0 0 0 1 0 0 0	Command Complete Sequence complete.

Sequence Step
Table 17

FIFO Flags   Read Address 07

The least significant 5 bits of this register
indicate how many bytes are currently in
the FIFO. The value is binary encoded.
The flags should not be polled while trans-
ferring data because they will not be stable
while the SCSI interface is changing the
contents of the FIFO.

FIFO Flags and
Sequence Step Register

(Normal Mode)

SS2	SS1	SS0	FF4	FF3	FF2	FF1	FF0
7	6	5	4	3	2	1	0

SS = Sequence Step   FF = FIFO Flag

Read Address 07
Figure 8

The upper three bits are duplicates of the
Sequence Step Register bits when opperat-
ing in normal mode.

If Test Mode is enabled, bit 5 is set to indi-
cate that the offset counter is not zero. Not
zero means that synchronous data may
continue to be transferred. Zero means that
the synchronous offset count has expired

and the ASC will not transfer any more data
until it receives an acknowledge.

Synchronous Offset   Write Address 07

The least significant four bits of this regis-
ter specify weather the ASC will transfer
Data Phase bytes synchronously or asyn-
chronously. **Zero specifies asyn-**
chronous transfer. Any other value
specifies the Synchronous Offset; the
number of Data Phase bytes that may be
sent synchronously without an acknowl-
edge (either REQuest or ACKnowledge,
depending on whether the ASC is in Initia-
tor or Target mode).

When transmitting to the SCSI bus, the
ASC will stop sending bytes when it
reaches this offset; and thereafter send one
byte for every acknowledge it receives from
the other SCSI device.

When receiving from the SCSI bus, the
ASC will send an acknowledge every time
a byte is removed from its FIFO on the
DMA (or host processor) interface. The
maximum offset of fifteen allows a receiv-
ing ASC to store data in its FIFO while the
external DMA controller gains control of
the memory bus.

The Synchronous Offset is cleared (0) by hardware RESET or software Reset Chip (but not SCSI reset).

Configuration-1 Register

This 8-bit read/write register specifies various operating conditions for the ASC. Any bit pattern written to this register may be read back and should be identical.

Configuration-1 Register

Slow	SRR	P Test	En P Chk	Chip Test	My Bus ID		
7	6	5	4	3	2	1	0

Read/Write Address 08
Figure 9
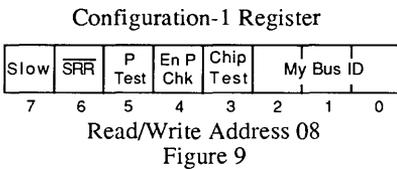
Bit 7   Slow Cable Mode

Slow Cable mode will seldom be necessary. It compensates for excessive capacitive loading on the SCSI data signals by inserting an extra CLK period between data being asserted on the bus and REQ or ACK being driven true. This bit is cleared (0) by hardware RESET or software Reset Chip (but not SCSI reset).

Bit 6   SCSI Reset Reporting Interrupt Disable

This bit disables the reporting of a SCSI reset. If the SCSI reset signal goes true when this bit is set, the ASC will disconnect from the SCSI bus and remain idle in the disconnected state without interrupting the host. If the bit is not set the ASC will respond to the SCSI reset by first interrupting the host, then resetting the host if the interrupt is not serviced within 1-2 mS (depending on CLK frequency and Clock Conversion Factor--see *Bus Initiated Reset*). This bit is cleared (0) by hardware RESET or software Reset Chip (but not SCSI reset).

Bit 5   Parity Test Mode

Setting this bit will cause the parity signal to be a duplicate of data bit 7 when unloading the FIFO to either the SCSI Bus or the host processor bus (53C90B only). This allows parity errors to be created so that hardware and software may be tested. This bit must not be set during normal operation. Also see *Parity Checking and Generation.* This bit is cleared (0) by hardware RESET or software Reset Chip (but not SCSI reset).

Bit 4   Enable Parity Checking

When this bit is set, the ASC will check parity on incoming SCSI bytes during any Information Transfer Phase except when receiving pad bytes. Detected parity errors will cause a bit to be set in the Status Register but will not cause an interrupt. In Initiator role, bad parity will also set ATN (Attention) on the SCSI bus. When this bit is not set, parity will not be checked; the bit in the Status register will not be set; and ATN will not be asserted. Also see *Parity Checking and Generation.* This bit is cleared (0) by hardware RESET or software Reset Chip (but not SCSI reset).

Bit 3   Chip Test Mode Enable

When this bit is set, the chip is placed in special test mode which enables the Test Register at address 0A hex. Once it has been set, the chip must be reset (hard or soft but not SCSI) before normal operation can begin. This bit should not be set during normal operation. This bit is cleared (0) by hardware RESET or software Reset Chip (but not SCSI reset).

Bit 2-0   My Bus ID

The Bus ID of this device. It is the ID to which the ASC responds during bus initiated Selection or ReSelection; and the ID that the ASC uses to arbitrate for the bus.

The name of this field has changed from Bus ID on the C90, but its function remains the same. This three bit field is binary encoded. It is not changed by any reset; after power-up the states of these bits are unpredictable.

**Clock Conversion**   Write address 09

This register must be set according to the CLK (clock) input frequency. All timings longer than 400 nS depend on this register correctly agreeing with the CLK frequency. The least significant three bits are binary encoded, and should be set to one of the four values below.

CLK Frequency (MHz)	Clock Conversion Factor
10	2
10.01 to 15	3
15.01 to 20	4
20.01 to 25	5

This register must never be loaded with 1. Hardware RESET or software Reset Chip will set the Clock Conversion Register to 2. SCSI reset will not affect it. The upper 5 bits of this register are reserved by NCR.

Test Register   Write Address 0A

This register is enabled by setting the special Test Mode bit in Config-1 at address 08. After Test Mode has been entered, a hardware RESET or software Reset Chip must occur before normal operation can begin.

Test Register

Reserved			Hi Z	I	T
7	6	5	4	3	2	1	0
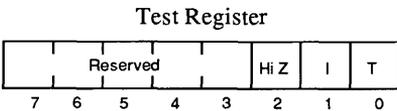
Write Address 0A
Figure 10

Bit 2   All Outputs to High Impedance

When this bit is set, all bidirectional and all output pins go to high impedance and will not significantly load a TTL or compatible device.

Bit 1   Initiator Mode

When this bit is set, the ASC is artificially forced into Initiator mode. Any Initiator command will be accepted by the ASC. For example, a Set ATN command will cause ATN to be driven on the SCSI bus even if the ASC is disconnected.

Bit 0   Target Mode

When this bit is set, the ASC is artificially forced into Target mode. Any Target command will be accepted by the ASC. For example, a DMA command will load or unload the FIFO and set the SCSI Phase, Data and REQ signals even if Arbitration and Selection have not occurred.

Configuration 2   R/W Address 0B

The 53C90A and 90B have a second configuration register that did not exist in the original C90. After hardware RESET or software Reset Chip, the bits in this register are all cleared, which makes the chip compatible with the older 53C90. Any bit pattern written to this register may be read back and should be identical.

Configuration-2 Register

Reserved		DREQ Hi Z	SCSI 2	BPA	RPE	DPE
7	6	5	4	3	2	1	0
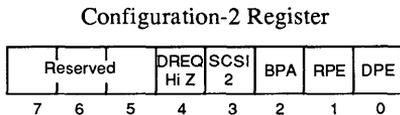
Read Write Address 0B
Figure 11

Bit 4   DREQ High Impedance

When this bit is set, the DREQ output (DMA Request) goes to high impedance and will not significantly load a TTL-compatible device. This is useful when several devices share the DMA Request line (known as wired-OR). When this bit is set, the ASC will ignore any activity on the DACK/ (DMA acknowledge) input.

When this bit is cleared, the DREQ output will be driven to TTL high or low voltages. When this bit is cleared, DACK/ is enabled to decrement the Transfer Counter and load or unload the FIFO, depending or WR/ or RD/. DACK/ should not pulse true without RD/ or WR/ because the Transfer Counter may decrement without transferring any data. See *Transfer Counter Register*.

Bit 3   SCSI-2

Allows the ASC to support two new features adopted in SCSI-2: the three-byte message exchange for Tagged-Queuing; and Group 2 Commands.

Tagged-Queuing

When this bit is set, and the ASC is selected with ATN (Attention) it will request either one or three Message bytes depending on whether ATN remains true or goes false. If ATN is still true after the first byte has been received, the ASC may request two more Message bytes before switching to Command Phase. If ATN goes false, it will request only one Message byte then switch to Command Phase. When the bit is not set it will request a single message byte (as a Target) when Selected with ATN; and abort the Selection sequence (as an Initiator) if the Target does not switch to Command Phase after one message byte has been transferred. Also see *Bus Initiated Selection*.

Group 2 Commands

When the SCSI-2 bit is set, Group 2 commands are recognized as 10-byte commands. Receiving a Group 2 command with this bit set will now set the Valid Group Code bit in the Status register. If the SCSI-2 bit is not set the ASC will treat Group-2 commands as Reserved Commands; it will request only 6 bytes in Command Phase and will not set the Valid Group Code Status bit.

Bit 2   Target Bad Parity Abort

When this bit is set, the ASC will abort a Receive Command or Receive Data sequence when the ASC detects a parity error.

Bit 1   Register Parity Enable

When this bit is set, parity from the host DBP pin (53C90B only) will be loaded into the FIFO when CS/ and WR/ are both true. When this bit is not set the ASC generates parity from the host data bus when CS/ and WR/ are both true and places it in the FIFO along with the data from which is was generated.

When the ASC is moving data from the FIFO to the SCSI bus, it will flag outgoing parity errors if either this bit or the DMA Parity Enable bit are set.

Bit 0   DMA Parity Enable

When this bit is set, parity from the host DBP pin (53C90B only) will be loaded into the FIFO when DACK/ and WR/ are both true. When this bit is not set the ASC generates parity from the host data bus when DACK/ and WR/ are both true and places it in the FIFO along with the data from which is was generated.

When the ASC is moving data from the FIFO to the SCSI bus, it will flag outgoing

parity errors if either this bit or the Register Parity Enable bit are set.

Parity Control			
Control Bit	Data Direction	Bit Set	Bit Not Set
Parity Checking Config-1 Bit 3	SCSI to FIFO	Enable Parity Checking and Error Reporting. SDPB loaded into FIFO.	Disable Parity Checking and Error Reporting. Parity generator to FIFO.
Test Parity Config-1 Bit 4	FIFO to SCSI	SDBP is replica of SDB7	FIFO to SDBP
	FIFO to Host	DBP is replica of DB7	FIFO to DBP
DMA Parity Config-2 Bit 0	DACK/ to FIFO	DBP to FIFO	Parity Generator to FIFO
	FIFO to SCSI	Enable Parity Checking and Error Reporting	Disable Parity Checking and Error Reporting
Register Parity Config-2 Bit 1	CS/ to FIFO	DBP to FIFO	Parity Generator to FIFO
	FIFO to SCSI	Enable Parity Checking and Error Reporting	Disable Parity Checking and Error Reporting

Parity Control
Table 18

PARITY CHECKING AND GENERATION

The ASC has four bits which control parity generation and checking. If Parity Checking is disabled, the ASC does not check for parity errors. In this document, the word *detected* in conjunction with *parity error* should be understood to imply that parity checking has previously been enabled. In Target Role, detected parity errors will set the Parity Error Status bit and clear the Command Register. In Initiator role, detected parity errors will set the Parity Error bit and assert ATN (Attention) prior to releasing ACKnowledge. Parity errors occurring on the first few bytes after a phase change to synchronous Data In are handled slightly differently in Initiator mode. See *Initiator Commands*.

If Parity Test Mode is enabled, the parity bit is a duplicate of bit 7. This is true both for data flowing from the FIFO to the SCSI Data Bus (SDB) or data flowing from the FIFO to the host Data Bus (DB).

The 53C90B has a parity pin (DBP) on the host bus. It may pass parity between SCSI and host busses without changing it or flagging errors; or may generate parity from the data byte. Whether generated internally, or externally, the parity bit is always loaded into the FIFO along with the data byte. From there on, it moves through the FIFO along with the byte. The FIFO may be accessed by three busses: SCSI bus, host processor bus or host DMA bus.

When checking parity, the ASC checks "at the edge of the board." Parity Errors are flagged as data comes into the FIFO from the SCSI bus, or as it leaves the FIFO on its way out to the SCSI bus.

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ASC COMMAND SET		
Command Register 7654 3210	**COMMAND MNEMONIC**	**Interrupt**
	MISCELLANEOUS GROUP	
x000 0000	NOP	no
x000 0001	Flush FIFO	no
x000 0010	Reset Chip	no
x000 0011	Reset SCSI bus	no*
	DISCONNECTED STATE GROUP	
x100 0000	Reselect sequence	yes
x100 0001	Select without ATN sequence	yes
x100 0010	Select with ATN sequence	yes
x100 0011	Select with ATN and stop sequence	yes
x100 0100	Enable selection/reselection	no
x100 0101	Disable selection/reselection	yes
x100 0110	Select with ATN3	yes
	TARGET STATE GROUP	
x010 0000	Send message	yes
x010 0001	Send status	yes
x010 0010	Send data	yes
x010 0011	Disconnect sequence	yes
x010 0100	Terminate sequence	yes
x010 0101	Target command complete sequence	yes
x010 0111	Disconnect	no
x010 1000	Receive message sequence	yes
x010 1001	Receive command	yes
x010 1010	Receive data	yes
x010 1011	Receive command sequence	yes
x000 0100	Target Abort DMA	no**
	INITIATOR STATE GROUP	yes
x001 0000	Transfer information	yes
x001 0001	Initiator command complete sequence	yes
x001 0010	Message accepted	yes
x001 1000	Transfer pad	no
x001 1010	Set ATN	

*The command itself does not cause an interrupt, however, external connection of
the RSTO/ pin to RSTI/ pin causes an interrupt if the SCSI Reset Reporting
is not disabled in the Configuration Register.

**The command itself does not cause an interrupt, however, it may allow a stalled
command to finish and generate an interrupt.

ASC Command Set
Table 19

COMMAND SET

From the programmers point of view, DMA commands will move data between memory and the SCSI bus; non-DMA commands will move data between the FIFO and the SCSI bus. Non-DMA commands require the host processor to move data between the FIFO and memory. DMA commands require an external DMA controller to move data between the FIFO and memory. A command with bit 7 set is a DMA command. A command with bit 7 not set is a non-DMA command. DMA commands will load the Transfer Counter with whatever value is in the Transfer Count Register--so the value must be correct before issuing the command.

MISCELLANEOUS COMMANDS		
DMA	NON-DMA	MNEMONIC
80	00	No Opperation (NOP)
81	01	Flush FIFO
82	02	Reset Chip
83	03	Reset SCSI Bus

Miscellaneous Commands
table 20

MISCELLANEOUS COMMANDS

NOP

No-Operation. The 53C90A and 53C90B require this command only after hardware RESET or software Reset Chip. A DMA NOP (80h) may be used to load the transfer counter with the value in Transfer Count Register. No Interrupt is generated from this command.

Flush FIFO

The Flush FIFO command initializes the FIFO to the empty condition by resetting the FIFO Flags and setting the bottom byte of the FIFO to zero.

Reset Chip

This command resets all functions in the chip and returns it to a disconnected state. The command has the same effect as a hardware reset, with the exception that Reset Chip cannot change between single-ended mode or differential mode.

Reset SCSI Bus

This command will assert the RSTO signal for 25 µS, depending on CLK frequency and Clock Conversion Factor (see *Bus Initiated Reset*). This command does not cause an interrupt, however, since RSTI will be externally connected to RSTO, an interrupt will be generated unless it is disabled in the Config-1 Register.

DISCONNECTED STATE COMMANDS

If any of the Disconnected State commands are received by the ASC when it is not in the Disconnected State, the command will be ignored, the Command Register will be cleared, and the ASC will generate an Illegal Command interrupt.

ReSelect Sequence

This command will cause the ASC Target to Arbitrate for the bus then enter ReSelection Phase when it wins arbitration. The Identify message, required by SCSI protocol, must either be placed in the FIFO by the host processor before issuing the command or must be transferred by DMA; which involves setting the Transfer Count to one and setting up the external DMA controller. In either case, the the Time-Out and Destination ID must have previously been set. The sequence will terminate early if a ReSelect Time-Out occurs. If it terminates normally, a ReSelect interrupt will occur.

DISCONNECTED STATE COMMANDS		
DMA	**NON-DMA**	**MNEMONIC**
C0	40	ReSelect Sequence
C1	41	Select without ATN Sequence
C2	42	Select with ATN Sequence
C3	43	Select with ATN and Stop Sequence
C4	44	Enable Selection or ReSelection
C5	45	Disable Selection and ReSelection
C6	46	Select with ATN3

Disconnected State Commands
Table 21

Select Without ATN Sequence

This command will cause the ASC Initiator to Arbitrate for the bus; enter Selection Phase when it wins; and send the Command Descriptor Block (CDB). The 6, 10 or 12 byte CDB must have either been placed in the FIFO previously by the host processor or must be transferred by DMA; which involves setting the Transfer Count to 6, 10 or 12 and programming the External DMA controller. In either case, the Time-Out and Destination Registers must have previously been set. This command terminates early if a ReSelection Time-Out occurs; or the Target does not assert Command Phase; or the Target removes Command Phase too early. If it terminates normally, a Function-Complete/Bus-Service interrupt will be generated.

Select With ATN Sequence

This command will cause the ASC Initiator to Arbitrate for the bus, Select a device with ATN true then send one Message Phase byte followed by 6, 10 or 12 Command Phase bytes. The message and command bytes must have either been placed in the FIFO by the host processor or must be transferred by DMA; which involves setting the Transfer Count to 7, 11 or 13 and programming the external DMA controller. In either case, the Time-Out and Destination

ID Registers must have previously been programmed. This command terminates early if: a Select Time-Out occurs; Target does not assert Message Phase followed by Command Phase; Target removes Command Phase early. If it completes normally, a Function-Complete and Bus-Service interrupt will be generated.

Select With ATN and Stop

This command should be used in place of the one above when multiple Message Phase bytes are to be sent. The command will Select a Target with ATN asserted; send one Message Phase byte; and generate a bus service interrupt and stop.

Enable Selection/ReSelection

After receiving this command, the ASC will respond to bus initiated Selection or ReSelection. A command that causes the ASC to Select or ReSelect will cancel this command; the command must be re-issued within 250 mS after the ASC disconnects to preserve ANSI recommended timings. If DMA is enabled, incoming information will be placed in memory. If DMA is not enabled, incoming information will remain in the FIFO.

Disable Selection/ReSelection

This command disables an earlier enable Selection/ReSelection command. If bus initiated Selection or ReSelection had not yet begun when this command is received by the ASC, it will generate a Function Complete Interrupt. If bus initiated Selection or ReSelection had already begun, this command (and every other command) will be ignored. Refer to the section *Bus Initiated Selection and Bus Initiated ReSelection*.

Select With ATN3 Sequence

This command is similar to the Select With ATN command, but sends three message bytes instead of one. It will cause the ASC Initiator to Arbitrate for the bus, Select a device with ATN true, send three Message Phase bytes, deassert ATN, then send 6, 10 or 12 Command Phase bytes. The message and command bytes must have either been placed in the FIFO by the host processor or must be transferred by DMA; which involves setting the Transfer Count to 7, 11 or 13 and programming the external DMA controller. In either case, the Time-Out and Destination ID Registers must have previously been programmed. This command terminates early if: a Select Time-Out occurs; Target does not assert Message Phase followed by Command Phase; Target removes Command Phase early. If it completes normally, a Function-Complete and Bus-Service interrupt will be generated.

INITIATOR COMMANDS

If the ASC is not in Initiator State when it receives any of these commands, the command will be ignored; an Illegal Command Interrupt will be generated; and the Command Register will be cleared. Refer to the section *Command Register*.

If BSY goes false while the ASC is connected as an Initiator, it will generate a Disconnected Interrupt. The interrupt output will occur 1.5 to 3.5 CLK cycles after BSY goes false.

When the ASC receives the last byte of a Message In Phase, it will leave ACKnowledge asserted on the bus to prevent the Target from sending any more bytes until the Initiator decides to accept or reject the message. For non-DMA commands, every byte is presumed to be the last byte. For DMA commands, the Transfer Counter signals the last byte.

If parity checking is enabled and the ASC detects a parity error while in Initiator mode, it will automatically assert ATN prior to de-asserting ACK for the byte which has the error. The one exception is after a phase change to Synchronous Data In, described below.

If the Synchronous Offset register is non-zero (synchronous) and the phase changes to Data In, the DMA interface is immediately disabled and the reporting of a parity error during Data In Phase is delayed. The phase change to Data In will: latch the FIFO Flags to indicate how many bytes were in the FIFO (these bytes will be lost); clear the FIFO; load the FIFO with the first Data In byte; generate an interrupt; and continue to load the FIFO with incoming Data In bytes as long as the Target sends them, but not more than the specified Offset. To continue receiving Data In bytes, the host processor would normally issue the Transfer Information Command to re-enable the DMA interface. If parity checking is enabled, and a parity error occurred on a previous input phase (Message In or Status) then the parity error flag will be set in the Status Register and ATN (Attention) will be set on the SCSI bus. If a parity error occurred during the Data In phase, the parity bit will not be set nor will ATN be asserted until after the ASC receives the subsequent Transfer Information Command.

INITIATOR COMMANDS

DMA	NON-DMA	MNEMONIC
90	10	Transfer Information
91	11	Initiator Command Complete Sequence
92	12	Message Accepted
98	18	Transfer Pad
9A	1A	Set ATN (Attention)

Initiator Commands
Table 22

Transfer Information

This command can be used to send or receive any Information Phase bytes, but is most often used for Data Transfer. For synchronous transfer, DMA must be used. The ASC will continue to Transfer Information until one of the following four terminating events occurs:

- Transfer is complete. This successful completion will create a Bus Service Interrupt. For a DMA Transfer Info, the transfer is complete when the Transfer Count decrements to zero and the FIFO is empty and the Target asserts REQuest for the next byte. For non-DMA Transfer Info in which the ASC is sending bytes to the SCSI bus, transfer is complete when the FIFO empties and the Target asserts REQuest for the next byte. For non-DMA Transfer Info in which the ASC is receiving bytes from the SCSI bus, transfer is complete after one byte is received and the Target asserts REQuest for the next byte. Thus non-DMA Transfer Info commands will generate an interrupt for every byte received.

If the phase is Message Out, the ASC removes ATN prior to asserting ACK for the last byte of the message. For non-DMA, every byte is assumed to be the last byte. For DMA, the transfer counter indicates the last byte.

- Target changes phase. The ASC clears the Command Register and generates a Bus Service Interrupt--after the Target asserts REQuest for the next byte.

- Target releases BSY (Busy). The ASC generates a Disconnected Interrupt.

- The ASC receives the last byte of a Message In Phase. (For non-DMA every byte is assumed to be the last byte. For DMA, the transfer counter signals the last byte.) The ASC leaves ACKnowledge asserted and generates a Function Complete Interrupt.

All Message In and Status Phase transfers are handled one byte at a time. If DMA is enabled, the next byte will not be received until the current byte has been written to buffer memory and the FIFO is empty. If DMA is not enabled, each byte will create an interrupt.

Initiator Command Complete Sequence

This command will cause the ASC to receive a Status byte followed by a Message byte. It terminates early if the Target does not assert Message In Phase, or if the Target disconnects. After receiving the Message byte, the ASC leaves ACKnowledge asserted on the bus to allow the Initiator to assert ATN if the message is unacceptable.

Message Accepted

This command releases the ACKnowledge signal on the SCSI bus. Any of the commands that receive bytes during Message Phase will leave ACK asserted after receiving the last message byte. To accept the message, issue this command. To reject the message, Set ATN then issue this command.

Transfer Pad

Transfer pad is usually an error recovery technique. It is useful when a Target requests more bytes than an Initiator has to send; or when an Initiator must receive and discard a number of bytes from a Target.

When transmitting to the SCSI bus, Transfer Pad will fill the FIFO with null-bytes and send them to the SCSI bus. When receiving from the SCSI bus, Transfer Pad will receive bytes, place them on the top of the FIFO and discard them from the bottom of the FIFO.

When sending pad bytes to the SCSI bus, DMA must be enabled. No DMA requests are actually made, but the ASC uses the transfer counter to end the transfer.

The command terminates under the same conditions as the Transfer Info command, except that the ASC does not leave ACK asserted on the last byte of a Message In Phase. If the command terminates early (due to phase change or disconnect) the FIFO may contain pad bytes.

Set ATN

This command asserts Attention on the SCSI bus. No interrupt is generated from this command. ATN stays asserted until the last byte of a Message Out Phase. DMA commands use the Transfer Counter to indicate the last byte. For non-DMA commands, every byte is assumed to be the

last byte. ATN will also be released if the Target prematurely disconnects.

TARGET COMMANDS

If the ASC receives any of these commands when it is not in Target State, it will ignore the command; clear the Command Register; and generate an Illegal Command interrupt; Refer to the section *Command Register*.

Normal completion of these commands will cause a Function Complete interrupt. If ATN is asserted, the Bus Service bit will be set in the Status Register. If the ASC was idle when ATN was asserted, a Bus Service Interrupt will be generated; the Function Complete bit will be zero; and the Command Register will be cleared.

Send Message

This command will cause the ASC to assert Message In Phase and send bytes until the FIFO is empty and the Transfer Counter is zero (if DMA).

Send Status

This command will cause the ASC to assert Status Phase and send bytes until the FIFO is empty and the Transfer Counter is zero (if DMA).

Disconnect Sequence

This command will cause the ASC to assert Message In Phase, send two bytes, then disconnect from the SCSI bus. Normally, the first byte will be a Save Data Pointers message and the second will be a Disconnect Message. If ATN is asserted by the initiator, the Bus Service and Function Complete bits will be set; an interrupt will be generated; but the ASC will not disconnect.

TARGET COMMANDS

DMA	NON-DMA	MNEMONIC
A0	20	Send Message
A1	21	Send Status
A2	22	Send Data
A3	23	Disconnect Sequence
A4	24	Terminage Sequence
A5	25	Target Command Complete Sequence
A7	27	Disconnect
A8	28	Receive Message Sequence
A9	29	Receive Command
AA	2A	Receive Data
AB	2B	Receive Command Sequence
84	04	Target Abort DMA

Target Commands
Table 23

Terminate Sequence

This command will cause the ASC to first assert Status Phase, send one byte; then assert Message In Phase and send one more byte. If ATN is asserted by the initiator, the Bus Service and Function Complete bits will be set; an interrupt will be generated; but the ASC will not disconnect.

Target Command Complete Sequence

This command is similar to Terminate Sequence, but is used for linked commands. It will cause the ASC to first assert Status Phase, send one byte; then assert Message In Phase and send one more byte. The message byte will normally be a Command Complete Message. If ATN is asserted by the initiator, the Bus Service and Function Complete bits will be set; an interrupt will be generated; but the ASC will not disconnect.

Disconnect

This command causes the ASC to release all SCSI bus signals except RSTO. The ASC returns to the disconnected state without generating an interrupt.

Receive Command

This command will cause the ASC to assert Command Phase and receive bytes from the Initiator. For non-DMA Receive Command, only one byte per interrupt may be received. DMA Receive Command will interrupt after the transfer counter decrements to zero.

Receive Data

This command will cause the ASC to assert Data Out Phase and receive bytes from the Initiator. For non-DMA Receive Data, only one byte per interrupt may be received. DMA Receive Data will interrupt after the transfer counter decrements to zero.

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Receive Command Sequence

This command will cause the ASC to assert Command Phase and receive a number of bytes, which will vary according to the the Group Code field of the first byte. If the SCSI-2 bit is set in the Config-2 register, Group 2 commands will be recognized as 10 byte commands. If the SCSI-2 bit is cleared, Group 2 commands will be recognized as Reserved commands. Groups 3 and 4 are always reserved. The ASC will request 6 bytes for reserved commands; six bytes for Group 6 Vendor Unique Commands; and 10 bytes for Group 7 Vendor Unique Commands.

Target Stop DMA

This command allows the host processor to stop a DMA data transfer command. The ASC must be in Target State when this command falls to the bottom of the Command FIFO or an Illegal Command interrupt will be generated. Target Stop DMA may only be used when all of the following are true.

1) Either a Target Send Data or Target Receive Data command are currently executing.

2) The DMA controller has stopped

3) The ASC is in *steady state*, ie:
   i Send data--the FIFO is empty

   ii Receive asynchronous data--the FIFO is full or the transfer counter is zero

   iii Receive sync data-- the transfer counter is zero or the Synchronous Offset Max bit (Read Register 06, bit 3) is not set.

Upon receiving this command, the ASC will reset the DMA interface (release DREQ) then terminate the current command. It will not generate its interrupt until the rest of the completion criteria are met.

1) Send asynchronous data--completes immediately

2) Send synchronous data--completes when the offset counter is zero.

3) Receive asynchronous data--completes immediately. There will be data in the FIFO which should be removed by the host processor.

4) Receive synchronous data--completes when all outstanding SCSI ACK's have been received. The Offset Counter is separate from the Transfer Counter. There will be data in the FIFO which should be removed by the host processor.

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D.C. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM STRESS RATINGS

Symbol	Parameter	Test Condition	Min	Max	Unit
Tstg	Storage Temperature		-55	150	°C
Vdd	Supply voltage		-0.5	7.0	V
Vin	Input voltage		Vss-0.5	Vdd+0.5	V
Ilp	Latch-Up Current	-2V < Vpin < +8V	±100		mA
ESD	Electrostatic Discharge	Human Body Model			
	SCSI pins	100 pF at 1.5 kΩ	±6000		V
	other pins	100 pF at 1.5 kΩ	±3000		V

Conditions that exceed the Absolute Maximum Stress limits may destroy the device. Conditions outside the Operating limits but within the Stress limits, may cause the device to function incorrectly.

OPERATING CONDITIONS

Symbol	Parameter	Test Condition	Min	Max	Unit
Vdd	Supply voltage		4.75	5.25	V
Idd	Supply current	Static *		10	mA
Idd	Supply current	Dynamic		50	mA
Ta	Ambient temperature		0	70	°C

* Static means: all inputs at Vss, all outputs floating, and all bidirectional pins configured as inputs.

Bi-Directional pins DB0-DB7, DBP

Symbol	Parameter	Test Condition	Min	Max	Unit
Vih	Input high voltage		2.0	Vdd+0.5	V
Vil	Input low voltage		Vss-0.5	0.8	V
Voh	Output high voltage	Ioh = -2 mA	2.4	Vdd	V
Vol	Output low voltage	Iol = 4 mA	Vss	0.4	V
Iil	Input current, low	Vin = Vil	-400	10	µA
Iih	Input current, high	Vin = Vih	-10	10	µA
Ipu	Hi-Z pull-up current		100	400	µA
CIO	Capacitance			12	pF

Non-SCSI Input Pins A3-A0, CS/, DACK/, RD/, WR, DIFFM, RESET, CLK

Symbol	Parameter	Test Condition	Min	Max	Unit
Vih	Input high voltage		2.0	Vdd+0.5	V
Vil	Input low voltage		Vss-0.5	0.8	V
Iin	Input leakage current	0 < Vin < Vdd	-400	10	µA
Cin	Capacitance			12	pF

SCSI Input Pins SDI7/-SDI0/, SELI/, BSYI/, REQI/, ACKI/ MSGI/, C/DI, I/OI, ATNI/, RSTI/

Symbol	Parameter	Test Condition	Min	Max	Unit
Vih	Input high voltage		2.0	Vdd+0.5	V
Vil	Input low voltage		Vss-0.5	0.8	V
Vh	Hysteresis		200		mV
Iil	Input low leakage	Vin = 0.5; 0 ≤ Vdd ≤ 5.5	-0.4	0.0	mA
Iih	Input high leakage	Vin = 2.7; 0 ≤ Vdd ≤ 5.5	0.0	0.1	mA
Cin	Capacitance			12	pF

Outputs

Symbol	Parameter	Test Condition	Min	Max	Unit
Cout	Capacitance			12	pF

DREQ, IGS

Symbol	Parameter	Test Condition	Min	Max	Unit
Voh	Output high voltage	Ioh = -2 mA	2.4	Vdd	V
Vol	Output low voltage	Iol = 4 mA	Vss	0.4	V
Ioz	Hi-Z state leakage	0 < VOUT < Vdd	-10	10	μA

INT/

Symbol	Parameter	Test Condition	Min	Max	Unit
Vol	Output low voltage	Iol = 4 mA	Vss	0.4	V
Ioz	Hi-Z state leakage	0 < Vout < Vdd	-10	10	μA

TGS, RESETO

Symbol	Parameter	Test Condition	Min	Max	Unit
Voh	Output high voltage	Ioh = -4 mA	2.4	Vdd	V
Vol	Output low voltage	Iol = 8 mA	Vss	0.4	V
Ioz	Hi-Z state leakage	0 < Vout < Vdd	-10	10	μA

RSTO/, SELO/, BSYO/, ATNO/, MSGO/, CDO/, IOO/, REQO/, ACKO/, SDO0-SDO7/, SDOP/

Symbol	Parameter	Test Condition	Min	Max	Unit
Vol	Output low voltage	Iol = 48 mA	Vss	0.5	V
Ioz	Hi-Z state leakage	0 < VOUT < Vdd	-10	10	μA
Tf	Fall time	SCSI termination	4		nS

A.C. ELECTRICAL CHARACTESTICS

The A.C. characteristics described in this section apply over the voltage range Vdd equal to 4.75 to 5.25 volts and the temperature range 0 to 70°C. Chip output timing is based on simulation under worst case conditions (4.75 V, 70°C) and the following pad termination:

| Test Conditions	
Signal Name	Output Load
RESETO, DREQ, TGS, IGS, SDIP/, SDI7/-SDI0/	50 pf
DB7...0	85 pf
INT/	50 pf 1K pullup
RSTO/, SELO/, BSYO/, ATNO/, MSGO/, CDO/ IOO/, REQO/, ACKO/, SDO7...0/, SDOP/	200 pf 110 pullup 165 pulldown

System Interface

All timings in this specification are taken from the 10% & 90% points with respect to the specified VOL & VOH of the waveforms.

Clock				
Symbol	Description	Min	Max	Unit
tcp	Clock period	40	100	ns
fcpa	Clock frequency, async	10*	25	MHz
fcps	Clock frequency, sync	12*	25	MHz
tch	Clock high	14.58		ns
tcl	Clock low	14.58		ns
tcs	Sync latency = tcp + tcl			

*Note: These minimum numbers required to comply with ANSI SCSI specification.
For synchronous SCSI data transfers, the Clock input must also meet the following requirements.

$2tcp + tcl \geq 97.92$ ns $2tcp + tch \geq 97.92$ ns

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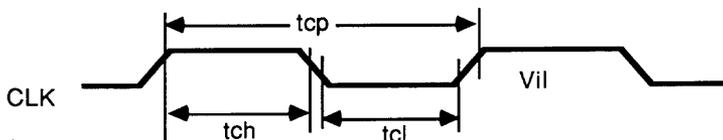
Reset Input				
Symbol	Description	Min	Max	Unit
trst	RESET pulse width	2tcp		ns
trh	RESET high to RESETO high		50	ns
trl	RESET low to RESETO low		50	ns
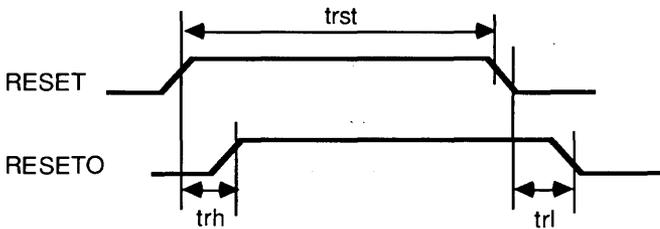
| Interrupt Output				
Symbol	Description	Min	Max	Unit
tir	INT/ to Interrupt Reg. RD/	0		ns
trd	RD/ pulse width	50		ns
tri	RD/ low to INT/ high		100	ns
ticy	RD/ high to INT/ low	tcs		ns

Notes:
1. Refer to the register read specification for the timing requirement of CS/, RD/, and A3..A0 for reading the Interrupt Status Register.
2. The Interrupt Status Register should not be read when INT/ is inactive.
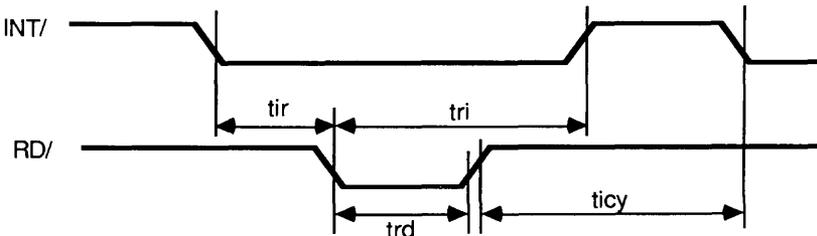
Register Write

Symbol	Description	53C90A Min	53C90A Max	53C90B Min	53C90B Max	Unit
trasc	Address setup to CS/	0		0		ns
trcsw	CS/ setup to WR/	0		0		ns
trwr	WR/ pulse width	40		40		ns
trdw	Data setup to WR/ high	15		15		ns
trahw	Address hold time from CS/	50		50		ns
trdhw	Data hold time from WR/	0		0		ns
trchw	WR/ high to CS/ high	0		50		ns
trccy	CS/ high to CS/ low	40		40		ns
trwcy	WR/ high to WR/ low	60		60		ns

Notes: 1. DACK/ must be inactive during all register I/O.
2. CS/ must be cycled to capture a new register address.
3. WR/ edges may precede or follow CS/ edges.
   If WR/ is held low, the data setup to CS/ high is 25 ns minimum;
   the data hold from CS/ high is 60 ns. min., and trccy is 60 ns min.
4. Trchw may be reduced to zero on 53C90B if certain parity control
   options are not required. Refer to SEN 819.
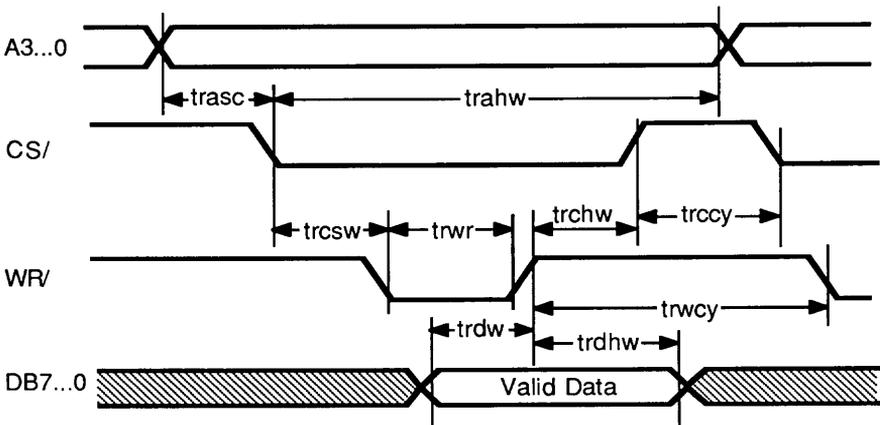
| Register Read				
Symbol	Description	Min	Max	Unit
trasc	Address setup to CS/	0		ns
trcsr	CS/ setup to RD/	0		ns
trrd	RD/ pulse width	50		ns
trdr	RD/ to data valid		50	ns
trdc	CS/ to data valid		70	ns
trahr	Address hold time from CS/	50		ns
trdhr	Data hold time	2	40	ns
trchr	RD/ high to CS/ high	0		ns
trrcy	CS/ high to CS/ low	40		ns

Notes:
1. DACK/ must be inactive during all register I/O.
2. CS/ must be cycled to capture a new register address.
3. RD/ edges may precede or follow CS/ edges.
    If RD/ is held low, the time from CS/ low to stable data is
    trdc and the data release time from CS/ high is trdhr.
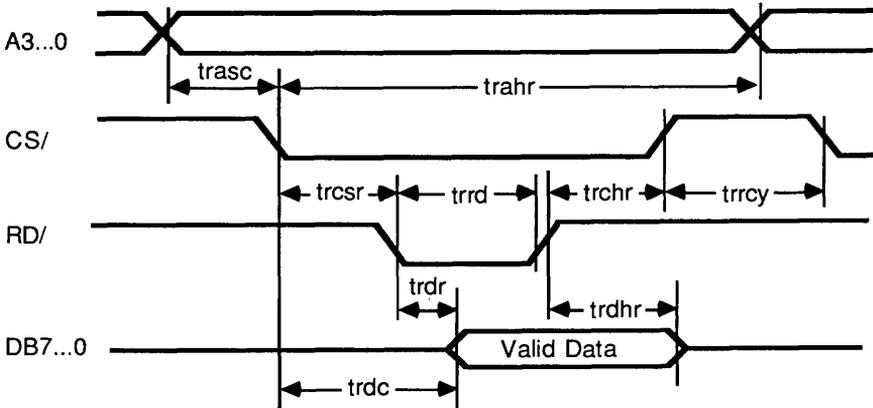
| DMA Write				
Symbol	Description	Min	Max	Unit
tdarl	DACK/ low to DREQ low (negation pending)	0	38	nS
tdaw	DACK/ low to WR/ low	0		nS
tdwr	WR/ pulse width	40		nS
tddw	Data to WR/ high	15		nS
tdwa	WR/ high to DACK/ high	0		nS
tdhw	Data hold time	0		nS
tdacy	DACK/ high to DACK/ low	12		nS
tdrh	DACK/ high to DREQ high (assertion pending)	0		nS
tdack	DACK/ pulse width	50		nS
tdwcy	WR/ high to WR/ low	40		nS

Notes: 1. CS/ must be inactive during all DMA accesses.
      2. DACK/ must be cycled once for each write access.
      3. WR/ edges may precede or follow DACK/ edges.
         If WR/ is held low, the data setup to DACK/ high is
         15 ns min, and tdacy is 40 ns min.
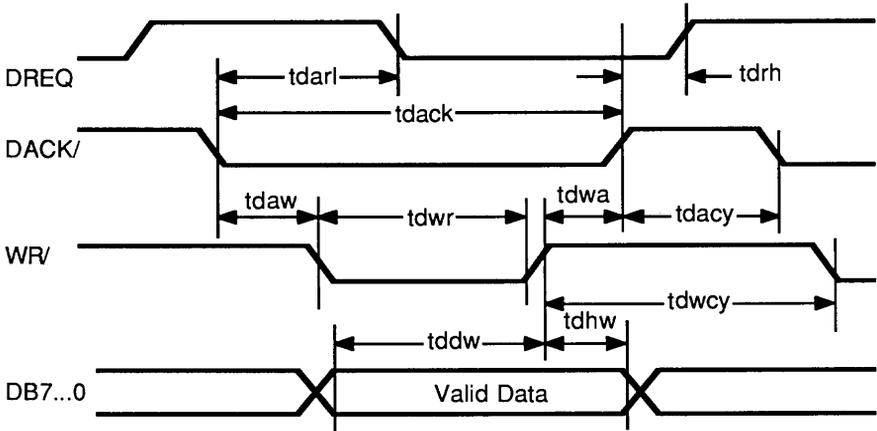
- For synchronous data transfers DACK/ low to DACK/ high must equal or exceed 2tcp and tcs +35 - tdacy.

- DREQ will remain true as long as the FIFO has room to receive at least one more byte. If the current write-cycle fills the FIFO, DREQ will go false. If the SCSI bus then removes a byte from the FIFO, DREQ will not go true until DACK/ goes false.

NCR

| DMA Read				
Symbol	Description	Min	Max	Unit
tdarl	DACK/ low to DREQ low (negation pending)	0	38	ns
tdar	DACK/ low to RD/ low	0		ns
tdrd	RD/ pulse width	50		ns
tddr	RD/ to data valid		41	ns
tdda	DACK/ to data valid		41	ns
tdra	RD/ high to DACK/ high	0		ns
tdhr	Data hold time	2	40	ns
tdacy	DACK/ high to DACK/ low	12		ns
tdrh	DACK/ high to DREQ high (assertion pending)	0		ns
tdack	DACK/ pulse width	50		ns

Note: 1. CS/ must be inactive during all DMA accesses.
2. DACK/ must be cycled once for each read access.
3. RD/ edges may precede or follow DACK/ edges.
   If RD/ is held low, the time from DACK/ low to stable data is tdda and the data release time is tdhr.
4. If tdacy ≤ 15 ns, then tdda is 45 ns max.
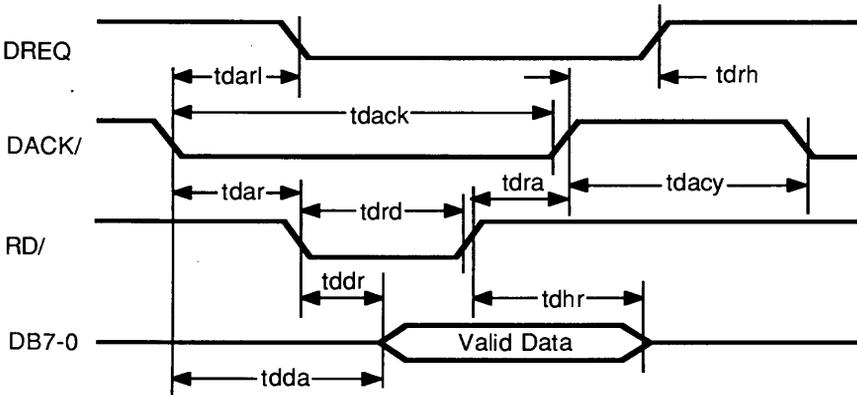
- For synchronous data transfers DACK/ low to DACK/ high must equal or exceed 2tcp and tcs + 35 - tdacy.

- DREQ will remain true if there are more bytes in the FIFO. If the current read-cycle empties the FIFO, DREQ will go false. If the SCSI bus then loads another byte into the FIFO, DREQ will not go true until DACK/ goes false.

Initiator Asynchronous Send

Symbol	Description	Min	Max	Unit
tiaxda	Data setup to ACKO/ low	55		ns
tiaxah	REQI/ high to ACKO/ high		43	ns
tiaxrd	REQI/ high to next data byte valid (FIFO bottom full)		75	ns
tiaxal	REQI/ low to ACKO/ low (data already setup)		47	ns

SDO/

ACKO/ tiaxda tiaxrd

REQI/ tiaxah tiaxal
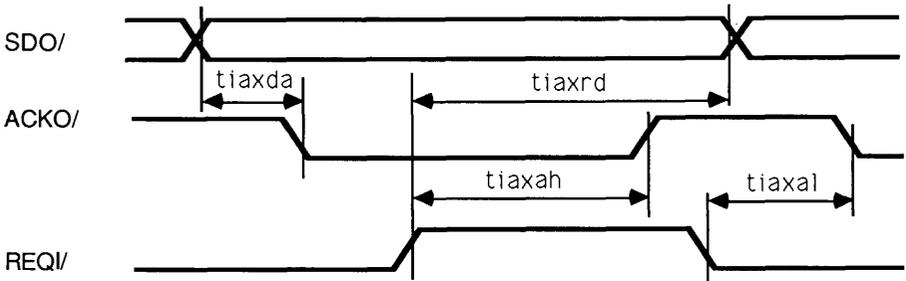
Initiator Asynchronous Receive

Symbol	Description	Min	Max	Unit
tiarah	REQI/ high to ACKO/ high		43	ns
tiaral	REQI/ low to ACKO/ low (FIFO not full)		47	ns

ACKO/

REQI/ tiarah tiaral
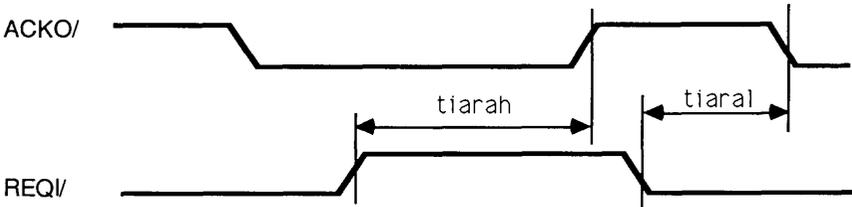
Target Asynchronous Send				
Symbol	Description	Min	Max	Unit
tTaxdr	Data setup to REQO/ low	55		ns
tTaxrh	ACKI/ low to REQO/ high		43	ns
tTaxad	ACKI/ low to next data byte valid		78	ns
	(FIFO bottom full)		45	ns
tTaxrl	ACKI/ high to REQO/ low			
	(data already set up)			

Target Asynchronous Receive				
Symbol	Description	Min	Max	Unit
tTarrh	ACKI/ low to REQO/ high		43	ns
tTarrl	ACKI/ high to REQO/ low		45	ns
	(FIFO not full)			

42
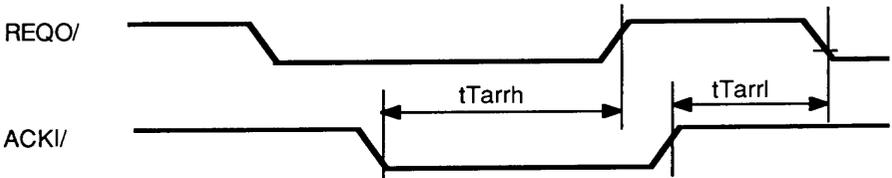
Target and Initiator Synchronous Transmit

Symbol	Description	Min	Max	Unit
tsxd	Data from CLK high		90	ns
tsxrl	REQO/ low from CLK high		70	ns
tsxrh	REQO/ high from CLK low		68	ns
tsxal	ACKO/ low from CLK high		70	ns
tsxah	ACKO/ high from CLK low		68	ns

CLK

SDO/

REQO/

ACKO/

Single-ended Mode without External Drivers

Host
Processor
and DMA
Interface

NCR 53C90A

SCSI
BUS

DB7	SDOP/	SDP/
DB6	SDO7/	SD7/
DB5	SDO6/	SD6/
DB4	SDO5/	SD5/
DB3	SDO4/	SD4/
DB2	SD03/	SD3/
DB1	SDO2/	SD2/
DB0	SDO1/	SD1/
CS/	SDO0/	SD0/
RD/	SDIP/	
WR/	SDI7/	
DREQ	SDI6/	
DACK/	SDI5/	
A3	SDI4/	
A2	SDI3/	
A1	SDI2/	
A0	SDI1/	
INT/	SDI0/	
RESET		
RESETO		
CLK	SELO/	SEL/
	BSYO/	BSY/
VDD	REQO/	REQ/
VDD	ACKO/	ACK/
	MSGO/	MSG/
VSS	CDO/	C/D/
VSS	IOO/	I/O/
VSS	ATNO/	ATN/
VSS	RSTO/	RST/
VSS	SELI/	
VSS	BSYI/	
	REQI/	
DIFFM	ACKI/	
	MSGI/	
	CDI/	
	IOI/	
	ATNI/	
	RSTI/	
	IGS	
	TGS	

+5V

1.0 – 25MHz CLK

+5V VDD
+5V VDD

GND VSS
GND VSS
GND VSS
GND VSS
GND VSS
GND VSS

GND DIFFM

44

SCSI BUS

SDP/ SD7/ SD6/ SD5/ SD4/ SD3/ SD2/ SD1/ SD0/

SEL/ BSY/ REQ/ ACK/ MSG/ C/D/ I/O/ ATN/ RST/

74ALS641A-1

A1 A2 A3 A4 A5 A6 A7 A8 DIR
B1 B2 B3 B4 B5 B6 B7 B8 C/ — GND
+5V

74ALS641A-1

A1 A2 A3 A4 A5 A6 A7 A8 DIR
B1 B2 B3 B4 B5 B6 B7 B8 C/ — GND
+5V

+5V Pull-Up 220Ω

+5V Pull-Up 220Ω

74AS760

74AS760

NCR 53C90A

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 CS/
RD/ WR/ DREQ DACK/ A3 A2 A1 A0 INT/
RESET
CLK
+5V VDD VDD
GND VSS VSS VSS VSS VSS VSS
GND DIFFM
GND

SDOP/ SDO7/ SDO6/ SDO5/ SDO4/ SDO3/ SDO2/ SDO1/ SDO0/
SDIP/ SDI7/ SDI6/ SDI5/ SDI4/ SDI3/ SDI2/ SDI1/ SDI0/
IGS
TGS
SELO/ BSYO/ REQO/ ACKO/ MSGO/ C/DO I/OO ATNO/ RSTO/
SELI/ BSYI/ REQI/ ACKI/ MSGI/ C/DI/ I/OI/ ATNI/ RSTI/

DMA Controller/ Processor Interface

+5V

10 - 25MHz

+5V +5V

GND GND GND GND GND GND GND

Differential Mode

.045 x 45° CHFR
.475
.050
.475
.350
.990
SQ.
.950
SQ.
PIN 1
INDICATOR
.028
.010 x 45° CHFR (3)
.083
.163
.018

.170
.150
.045 x 45° CHFR
.910
SQ.
.025
.108

68 Pin PLCC Package
Mechanical Drawing

47

Notes

NCR MICROELECTRONICS
1635 Aeroplaza Drive
Colorado Springs, CO 80916
(303) 596-5612, (800) 525-2252

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West Germany
(49) 89 632 03

ASIC/PACIFIC
2501, Vicwood Plaza
199 Des Voeux Road
Central
Hong Kong
852-5-452-406

Notes